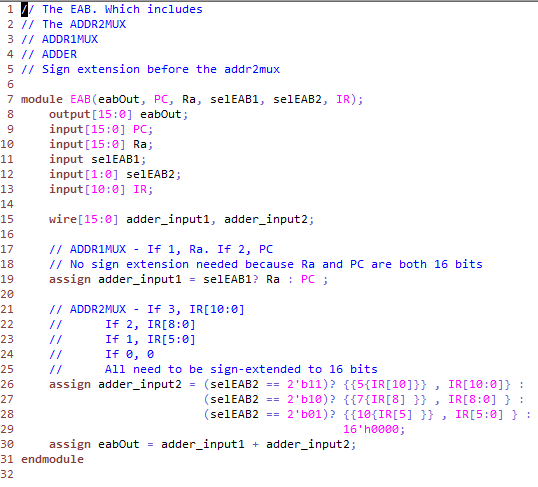
Taylor Cowley

Lab 10: Designing the LC3 Datapath (LC3 Functional Units)

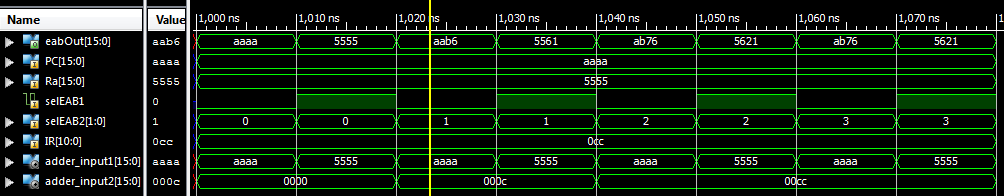
Why do these labs have 2 separate titles?

June 13 2016

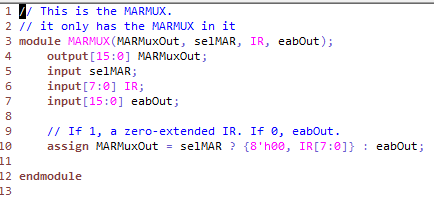
EAB Verilog file



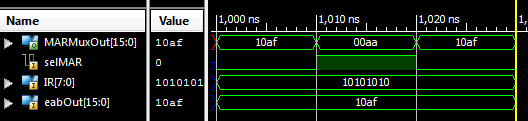
EAB Simulation waveform



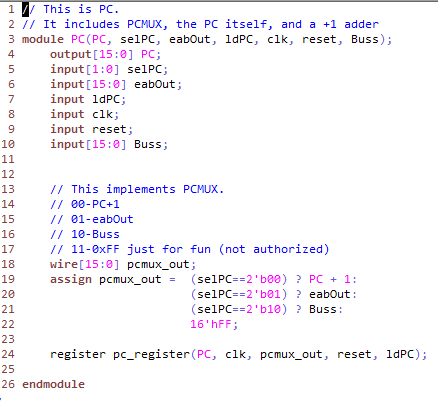
MARMux Verilog file



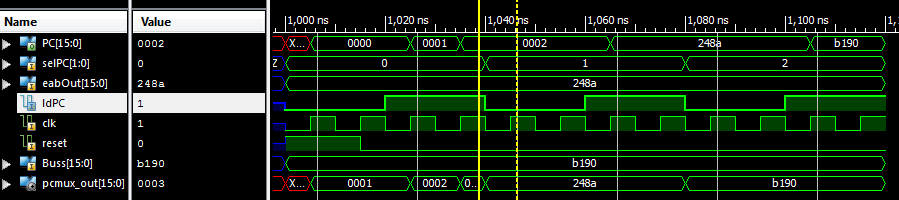
MARMux Simulation waveform



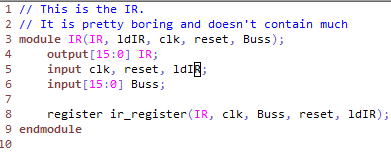
PC Verilog file



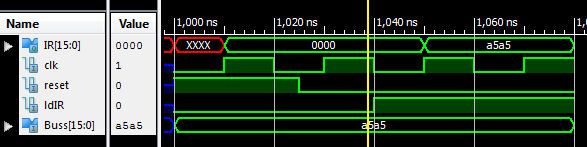
PC Simulation waveform



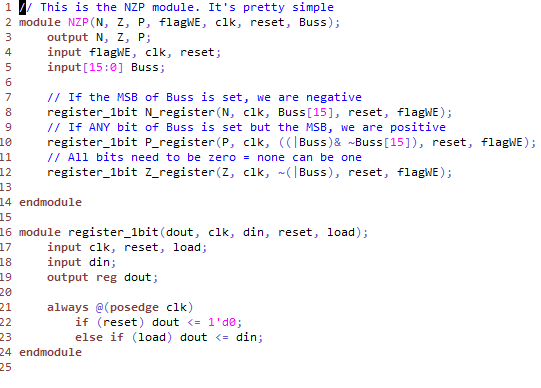
IR Verilog file



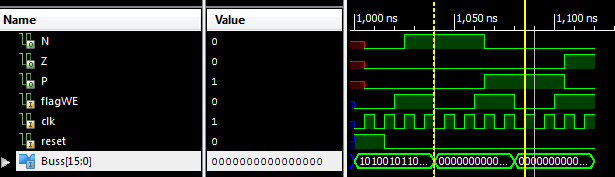
IR Simulation waveform



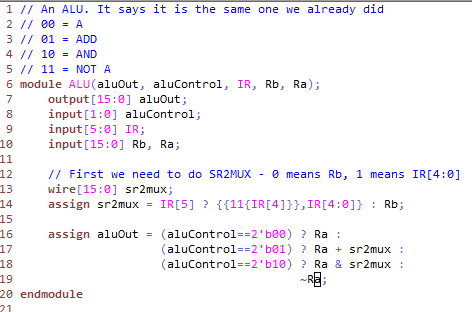
NZP Verilog file



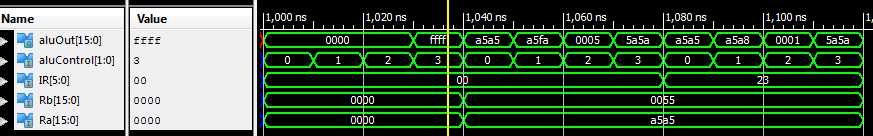
NZP Simulation waveform



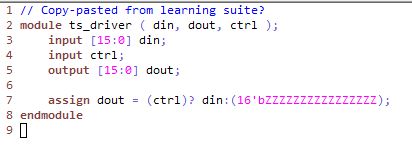
ALU Verilog file



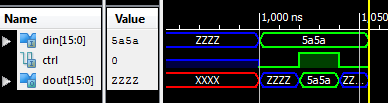
ALU Simulation waveform



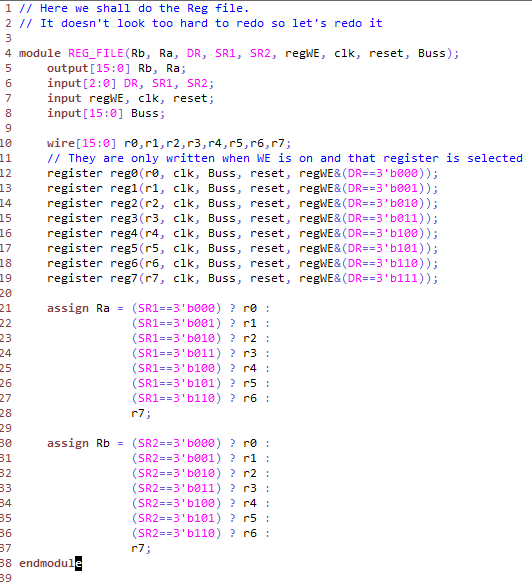
ts\_driver Verilog file



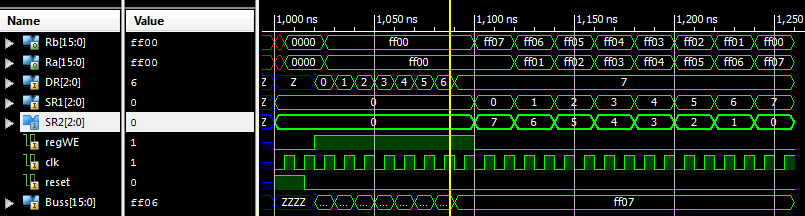
ts\_driver Simulation waveform



RegFile Verilog file



RegFile Simulation waveform



**Anomalies (bugs, problems, and suggestions)(5pts possible)**

So just realizing that I had to trust the basic modules- they aren’t doing anything special! Then it was easy to code up. And VIM is much nicer to code Verilog into than the Xilinx editor. In case you were wondering.